

PRELIMINARY AMENDMENT

Serial Number: Unknown

Filing Date: Herewith

Title: LOW ANGLE, LOW ENERGY PHYSICAL VAPOR DEPOSITION OF ALLOYS

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cont'd  
69. The integrated circuit of claim 65 where the silicide has at least two different stoichiometries.

70. The integrated circuit of claim 65 where the insulator has a top surface free of the silicide.

REMARKS

The modifications to the Specification numbered 2-6 and 8-22 above were previously entered in the parent patent application Serial No. 08/677,659 in response to an Examiner's Amendment to the Record, Paper #6, mailed September 29, 1997, by Examiner Aaron Weisstuch. The remaining modifications to the Specification represent typographical, grammatical, clerical or editorial modifications, and do not introduce new matter that would be prohibited by 35 USC 132.

The uniform stoichiometry recited in claims 36 and 68 is mentioned, inter alia, on page 7 line 25 of the Specification. Minimal consumption of the substrate by the material of the planar layer is discussed on page 15 line 1. Aspect ratios of the hole, specified in claims 39-41, are found on page 8 lines 11-14. Figs. 3a and 3b show the material in the layer at the bottom of the hole being confined thereto, and not extending substantially up the sidewalls, as recited in claims 42, 47, 53, and 57. Thickness variation of the bottom layer, as recited in claims 43-45 and 63-64, is described on page 14 lines 19-24. That the layer contacts the sidewalls, claims 46 and 52, is

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found on line 29 of the same page. Different stoichiometries, recited in claims 48 and 69, is found on page 15 lines 19-28. The particular insulator materials of claims 56 and 61 are discussed on page 8 lines 10-11. Removal of the material deposited in the bottoms of the contact holes from other areas of the integrated circuit is mentioned on page 14 lines 25-27.

Respectfully submitted,

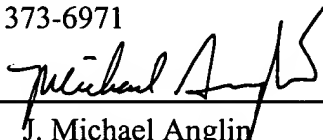
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